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EXAMINER	
KNOLL, CLIFFORD H	

ART UNIT	PAPER NUMBER
2112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/920,825	LEE, JIN WOO	
	Examiner	Art Unit	
	Clifford H Knoll	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is responsive to communication filed 5/14/2004. Currently claims 1-24 are pending.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

Claims 17-19 and 22-24 stand rejected under 35 U.S.C. 102(e) as being anticipated by Jung (US 6389554).

Regarding claim 17, Jung discloses a first device and a second device of the duplex device each having a D-channel controller and a C-channel controller; a D-channel interconnecting the D-channel controllers of the first and second devices to convey at least one of data signals, address signals, and control signals (e.g., Figure 3, "DATA CHANNEL"); and a C-channel interconnecting the C-channel controllers of the first and second devices to convey status signals, wherein the C-channel controller of the first and second devices each monitor a subset of the C-channel status signals to determine which of the first and second devices has an active mode status and which has a standby mode status, and both the active mode status and the standby mode status are identified by a self-side normal signal and a pair-side active signal (e.g., col. 7, lines 51-58).

Regarding claim 18, Jung also discloses the active mode status is identified by a true state existing on the self-side normal signal and a false state existing on the pair-side active signal, and the standby mode status is identified by other combinations of the true and false states existing on the self-side normal and pair-side active signals (e.g., col. 7, lines 51-58).

Regarding claim 19, Jung also discloses whichever one of the first and second devices that has the active mode status, generates the address signals conveyed by the D-channel (e.g., col. 8, lines 50-58).

Regarding claim 22, Jung discloses reading a first status of the first device and a second status of the second device; setting one of the first and second devices to an active mode status and the other of the respective devices to a standby mode status based on the first and second status, wherein both the first status and the second status are identified by a self-side normal signal and a pair-side active signal (e.g., col. 8, lines 50-58).

Regarding claim 23, Jung also discloses the active mode status is identified by a true state existing on the self-side normal signal and a false state existing on the pair-side active signal, and the standby mode status is identified by other combinations of the true and false states existing on the self-side normal and pair-side active signals (e.g., col. 8, lines 50-58).

Regarding claim 24, Jung also discloses the first and second devices each have a communication processing unit, a central processor, a memory, and a D-channel controller, which share both a common address bus and a common data bus; the first and second devices each have a C-channel controller that

communicates with the central processor of the respective first and second devices; a D-channel interconnects the D-channel controllers of the first and second devices to convey data signals, address signals, and control signals; and a C-channel interconnects the C-channel controllers of the first and second devices to convey the first and second status between the first and second C-channel controllers, wherein one of the first and second devices has the active mode status to generate the address signals conveyed by the D-channel and to control a read access and a write access to the memories of both the first and second devices (e.g., Figure 3).

Claims 1-3, 5, 7-24 stand rejected under 35 U.S.C. 102(e) as being anticipated by Chan (US 2001/0016920).

Regarding claim 1, Chan discloses the active module having a primary central processing unit that carries out control and data processes, a primary arbiter that arbitrates the use of a primary bus, a primary memory controller that controls access to a primary memory (e.g., paragraph [0029]), a primary D-channel controller that provides a primary first-in first-out (FIFO) memory for the communication of parallel data on a duplexing path (e.g., paragraph [0044]), and a primary C-channel controller that communicates primary status information of the active module (e.g., Figure 5A, "248A"), a standby module having a secondary central processing unit that carries out control and data processes, a secondary arbiter that arbitrates the use of a secondary bus, a secondary memory controller that controls access to a secondary memory (e.g., Figure 4), a

secondary D-channel controller that provides a second FIFO memory for the communication of the parallel data on the duplexing path (e.g., paragraph [0044]), and a secondary C-channel controller that communicates secondary status information of the standby module (e.g., Figure 5B, "248B"); a C-channel that exchanges the primary and secondary status information between the primary and secondary C-channel controllers to support duplexing logic between the active module and the standby module (e.g., Figures 5A, 5B); and a D-channel that supports access to the primary and secondary memories by both the primary and secondary central processing units (e.g., paragraph [0044]).

Regarding claim 2, Chan also discloses wherein each of the primary and secondary C-channel controllers identifies the primary status information and the secondary status information, based on the values of a self-side active signal, a self-side normal signal, a pair-side active signal, and a pair-side normal signal, and determines which one of the active and standby modules is operating in an active mode and which is operating in a standby mode (e.g., paragraph [0047]).

Regarding claim 3, Chan also discloses the self-side active signal transmitted by the primary C-channel controller is designated as the pair-side active signal, when received by the secondary C-channel controller; the self-side normal signal transmitted by the primary C-channel controller is designated as the pair-side normal signal, when received by the secondary C-channel controller; the self-side active signal transmitted by the secondary C-channel controller is designated as the pair-side active signal, when received by the primary C-channel controller (e.g., paragraph [0047]); and the self-side normal

signal transmitted by the secondary C-channel controller is designated as the pair-side normal signal, when received by the primary C-channel controller (e.g., paragraph [0050]).

Regarding claim 5, Chan discloses reading a secondary status of a secondary module, via a C-channel, with a primary module, comparing the secondary status with a primary status of the primary module to obtain a first result, determining a direction of a D-channel based upon the value of the first result, and determining which one of the primary and secondary modules is an active module based upon the value of the first result (e.g., paragraph [0047]), reading only the contents of a first memory in the active module to a processor within the active module that requested the contents, when the processor performs a memory read operation of the first memory, and concurrently writing data to the first memory and to a second memory in the one of the primary and secondary modules that is not the active module and is, therefore, designated a standby module, when the processor performs a memory write operation (e.g., paragraph [0040]), and recognizing, with the standby module, that a fault has occurred in the active module by identifying an abnormal signal communicated by a C-channel controller of the active module, changing the active module to a standby mode of operation, changing the standby module to an active mode of operation, changing the primary module or the secondary module that has the active mode of operation to be the active module, and changing the primary module or the secondary module that has the standby mode of operation to be the standby module (e.g., paragraph [0047]).

Regarding claim 7, Chan also discloses wherein step (b) further comprises: analyzing a transfer type signal and an address in a first D-channel controller of the active module to obtain a second result; if the second result is determined to be the memory read operation addressed to the first memory, reading the addressed contents only from the first memory and if the second result is determined to be either the memory write operation or the memory read operation addressed to the second memory, writing the address, the transfer type signal, and a transfer size signal from a first FIFO memory of the first D-channel controller to a second FIFO memory of a second D-channel controller of the standby module (e.g., paragraph [0066]); when an empty flag signal is asserted from the second FIFO memory, sending a bus request signal from the second D-channel controller to a bus arbiter of the standby module and receiving a bus grant signal at the second D-channel controller from the bus arbiter; after the bus grant signal is received, generating a transfer start signal from the second D-channel controller to a second memory controller of the standby module and transmitting the address to the second memory via an internal bus operation of the standby module; and if an operation completion signal is generated from the second memory controller, returning the bus grant signal to the bus arbiter (e.g., paragraph [0066], "slave data buffer 229B is not enabled until ...").

Regarding claim 8, Chan also discloses wherein the first FIFO memory writes the address, the transfer type signal and the transfer size signal to the

second FIFO memory during the memory read operation (e.g., paragraph [0072], "address and control buffers 231, 233").

Regarding claim 9, Chan also discloses wherein the address determines whether the contents are read from the first memory or the second memory (e.g., paragraph [0072], "262B").

Regarding claim 10, Chan also discloses a first memory address region common to both the first memory and the second memory and a second address region used only for reading from the second memory (e.g., paragraph [0040], "224A has the capability to read from the remote memory 234B").

Regarding claim 11, Chan also discloses wherein the first D-channel controller recognizes both the memory read operation having the second region address and the transfer type signal and converts the second region address into a corresponding first region address and writes the corresponding first region address to the second FIFO memory (e.g., paragraph [0040], "executes the memory write concurrently").

Regarding claim 12, Chan also discloses wherein the first FIFO memory, at the time of the memory write operation, writes the address, the transfer type signal and the transfer size signal to the second FIFO memory and the second D-channel controller transmits the address via an internal bus of the standby module (e.g., paragraph [0040]).

Regarding claim 13, Chan also discloses if the memory read operation or the memory write operation is completed abnormally, the second D-channel controller inputs a transfer error acknowledge signal and asserts a D-channel

error signal to the first D-channel controller, thereby generating a D-channel interrupt signal to the active module (e.g., paragraph [0051]).

Regarding claim 14, Chan also discloses if the memory read operation from the second memory is completed normally, the first D-channel controller communicates a primary transfer completion message to a first memory controller of the active module and the second D-channel controller communicates a secondary transfer completion message to the second memory controller (e.g., paragraph [0074]).

Regarding claim 15, Chan also discloses if the memory write operation to the second memory is completed normally, the second D-channel controller informs the first D-channel controller of a write completion (e.g., paragraph [0074]).

Regarding claim 16, Chan also discloses where step (c) further comprises: generating an interrupt in the active module, if the fault occurs; if the interrupt is generated in the active module, writing register information of a first D-channel controller, during a delay time, to a second FIFO memory of a second D-channel controller in a burst mode; if the write operation in the burst mode is completed, asserting a self-side abnormal status and a first self-side active status of the C-channel controller of the active module to a high state and transmitting an assert signal to the second D-channel controller; and asserting a second self-side active signal of the standby module to a low state; and changing the standby module to the active mode of operation (e.g., paragraph [0077]).

Regarding claim 17, Chan discloses a first device and a second device of the duplex device each having a D-channel controller and a C-channel controller; a D-channel interconnecting the D-channel controllers of the first and second devices (e.g., Figure 4), to convey at least one of data signals, address signals, and control signals (e.g., Figure 6, "229A"); and a C-channel interconnecting the C-channel controllers of the first and second devices to convey status signals, wherein the C-channel controller of the first and second devices each monitor a subset of the C-channel status signals to determine which of the first and second devices has an active mode status and which has a standby mode status, and both the active mode status and the standby mode status are identified by a self-side normal signal and a pair-side active signal (e.g., paragraph [0047]).

Regarding claim 18, Chan also discloses the active mode status is identified by a true state existing on the self-side normal signal and a false state existing on the pair-side active signal, and the standby mode status is identified by other combinations of the true and false states existing on the self-side normal and pair-side active signals (e.g., paragraph [0047]).

Regarding claim 19, Chan also discloses whichever one of the first and second devices that has the active mode status, generates the address signals conveyed by the D-channel (e.g., paragraph [0044]).

Regarding claim 20, Chan also discloses each of the first and second devices share a common address bus and a common data bus and further comprises: a communication processor that communicates input and output I/O) information between the duplex device and external devices; a central

processing unit that controls communication processes within the respective first and second devices; a memory that stores retained information; an arbiter that arbitrates the use of the common data bus, wherein one of the first and second devices has the active mode status to generate the address signals conveyed by the D-channel and to control a read access and a write access to each memory of the first and second devices (e.g., Figure 6, paragraph [0033]).

Regarding claim 21, Chan also discloses within both of the first and second devices, respectively, the communication processor, the central processing unit, the memory, and the D-channel controller share the common data bus and the common address bus (Figure 6).

Regarding claim 22, Chan also discloses reading a first status of the first device and a second status of the second device; setting one of the first and second devices to an active mode status and the other of the respective devices to a standby mode status based on the first and second status, wherein both the first status and the second status are identified by a self-side normal signal and a pair-side active signal (e.g., paragraph [0047]).

Regarding claim 23, Chan also discloses the active mode status is identified by a true state existing on the self-side normal signal and a false state existing on the pair-side active signal, and the standby mode status is identified by other combinations of the true and false states existing on the self-side normal and pair-side active signals (e.g., paragraph [0047]).

Regarding claim 24, Chan also discloses the first and second devices each have a communication processing unit, a central processor, a memory, and

a D-channel controller, which share both a common address bus and a common data bus; the first and second devices each have a C-channel controller that communicates with the central processor of the respective first and second devices; a D-channel interconnects the D-channel controllers of the first and second devices to convey data signals, address signals, and control signals; and a C-channel interconnects the C-channel controllers of the first and second devices to convey the first and second status between the first and second C-channel controllers, wherein one of the first and second devices has the active mode status to generate the address signals conveyed by the D-channel and to control a read access and a write access to the memories of both the first and second devices (e.g., Figure 4).

Claim Rejections - 35 USC § 103

Claims 1-3, 5 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Jung in view of standard PCI bus master practice, as further evidenced by Hammersley (US 6618783).

Regarding claim 1, Jung discloses an active module having a primary central processing unit that carries out control and data processes, a primary bus, a primary memory controller that controls access to a primary memory (e.g., col. 5, lines 43-46) , a primary D-channel controller that provides a primary first-in first-out (FIFO) memory for the communication of parallel data on a duplexing

path, and a primary C-channel controller that communicates primary status information of the active module (e.g., col. 3, lines 11-12); a standby module having a secondary central processing unit that carries out control and data processes, a secondary bus, a secondary memory controller that controls access to a secondary memory (e.g., col. 5, lines 46-51), a secondary D-channel controller that provides a second FIFO memory for the communication of the parallel data on the duplexing path (e.g., col. 3, lines 11-12), and a secondary C-channel controller that communicates secondary status information of the standby module; a C-channel that exchanges the primary and secondary status information between the primary and secondary C-channel controllers to support duplexing logic between the active module and the standby module (e.g., col. 7, lines 51-58). Jung does not expressly mention the particular detail of arbitration on primary and secondary buses, however the Examiner takes Official Notice that arbitration is a well-known aspect of interfacing a bus bridge, such as that of Jung to a PCI bus, as further evidenced by Hammersley. Hammersley discloses the necessity of arbitration for a PCI bridge (e.g., col. 1, lines 49-54). It would be obvious to combine the arbitration methods with Jung because arbitration is a well-known aspect of interfacing a PCI bridge. Therefore it would be obvious to one of ordinary skill in the art at the time the invention was made to combine standard PCI interface methods with Jung to obtain the claimed invention.

Regarding claim 2, Jung also discloses where each of the primary and secondary C-channel controllers identifies the primary status information and the secondary status information, based on the values of a self-side active signal, a

self-side normal signal, a pair-side active signal, and a pair-side normal signal, and determines which one of the active and standby modules is operating in an active mode and which is operating in a standby mode (e.g., col. 7, lines 51-58).

Regarding claim 3, Jung also discloses the self-side active signal transmitted by the primary C-channel controller is designated as the pair-side active signal, when received by the secondary C-channel controller; the self-side normal signal transmitted by the primary C-channel controller is designated as the pair-side normal signal, when received by the secondary C-channel controller; the self-side active signal transmitted by the secondary C-channel controller is designated as the pair-side active signal, when received by the primary C-channel controller; and the self-side normal signal transmitted by the secondary C-channel controller is designated as the pair-side normal signal, when received by the primary C-channel controller (e.g., col. 8, lines 50-63).

Regarding claim 5, Jung discloses reading a secondary status of a secondary module, via a C-channel, with a primary module, comparing the secondary status with a primary status of the primary module to obtain a first result determining a direction of a D-channel based upon the value of the first result, and determining which one of the primary and secondary modules is an active module based upon the value of the first result (e.g., col. 8, lines 50-57), reading only the contents of a first memory in the active module to a processor within the active module that requested the contents, when the processor performs a memory read operation of the first memory, and concurrently writing data to the first memory and to a second memory in the one of the primary and

secondary modules that is not the active module and is, therefore, designated a standby module, when the processor performs a memory write operation (e.g., col. 7, lines 42-50), and recognizing, with the standby module, that a fault has occurred in the active module by identifying an abnormal signal communicated by a C-channel controller of the active module, changing the active module to a standby mode of operation; changing the standby module to an active mode of operation; changing the primary module or the secondary module that has the active mode of operation to be the active module and changing the primary module or the secondary module that has the standby mode of operation to be the standby module (e.g., col. 1, lines 48-53, col. 10, lines 42-45).

Claims 20-21 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Jung as applied in claim 18 above, further in view of standard PCI bus master practice, as further evidenced by Hammersley (US 6618783).

Regarding claim 20, Jung also discloses each of the first and second devices share a common address bus and a common data bus and further comprises: a communication processor that communicates input and output I/O) information between the duplex device and external devices; a central processing unit that controls communication processes within the respective first and second devices; a memory that stores retained information, wherein one of the first and second devices has the active mode status to generate the address signals conveyed by the D-channel and to control a read access and a write access to each memory of the first and second devices (e.g., Figure 3). Jung

does not expressly mention the particular detail of arbitration on primary and secondary buses, however the Examiner takes Official Notice that arbitration is a well-known aspect of interfacing a bus bridge, such as that of Jung to a PCI bus, as further evidenced by Hammersley. Hammersley discloses the necessity of arbitration for a PCI bridge (e.g., col. 1, lines 49-54). It would be obvious to combine standard arbitration practice with Jung because arbitration is a well-known aspect of interfacing a PCI bridge. Therefore it would be obvious to one of ordinary skill in the art at the time the invention was made to combine standard PCI interface methods with Jung to obtain the claimed invention.

Regarding claim 21, Jung also discloses within both of the first and second devices, respectively, the communication processor, the central processing unit, the memory, and the D-channel controller share the common data bus and the common address bus (e.g., Figure 3).

Claims 4 and 6 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Jung, as applied to claims 2 and 5 respectively, above, and further in view of standard bus master embodiment, as further evidenced by of Shaffer (US 5884051).

Regarding claim 4, Jung also discloses each of the primary and secondary D-channel controllers obtains the primary status information and secondary status information, from the primary or secondary C-channel controller of its respective one of the active or standby modules and executes a duplexing

operation, as a master or a slave, in a communication direction of the D-channel determined by a comparison of the primary status information and the secondary status information (e.g., col. 8, lines 50-55). While Jung does not expressly mention a particular embodiment of the power PC (PPC) bus, the Examiner takes Official Notice that this is a well-known bus master standard as further evidenced by Shaffer. Shaffer discloses the well-known power PC bus (e.g., col. 4, lines 51-55, Figure 1). It would be obvious to combine the power PC bus with Jung, because the power PC bus is well-known bus master standard, and well recognized alternative embodiment of such. Therefore it would be obvious to one of ordinary skill in the art to combine a particular bus standard with Jung at the time the invention was made to obtain the claimed invention.

Regarding claim 6, Jung also discloses where the active module executes the memory write operation to the second memory, via the D-channel, and each of a primary D-channel controller and a secondary D-channel controller executes a duplexing operation, while serving as a master or slave in a bus mastering bus (e.g., col. 5, lines 28-33). While Jung does not expressly mention a particular embodiment of the power PC (PPC) bus, the Examiner takes Official Notice that this is a well-known bus master standard as further evidenced by Shaffer. Shaffer discloses the well-known power PC bus (e.g., col. 4, lines 51-55, Figure 1). It would be obvious to combine the power PC bus with Jung, because the power PC bus is well-known bus master standard, and well recognized alternative embodiment of such. Therefore it would be obvious to one of ordinary

skill in the art to combine a particular bus standard with Jung at the time the invention was made to obtain the claimed invention.

Claims 4 and 6 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Chan as applied to claims 3 and 5, respectively, above, and further in view of standard bus master embodiment, as further evidenced by of Shaffer.

Regarding claim 4, Chan also discloses wherein each of the primary and secondary D-channel controllers obtains the primary status information and secondary status information, from the primary or secondary C-channel controller of its respective one of the active or standby modules and executes a duplexing operation, as a master or slave in a communication direction of the D-channel determined by a comparison of the primary status information and the secondary status information (e.g., paragraph [0045]). While Chan does not expressly mention a particular embodiment of the power PC (PPC) bus, the Examiner takes Official Notice that this is a well-known bus master standard as further evidenced by Shaffer. Shaffer discloses the well-known power PC bus (e.g., col. 4, lines 51-55, Figure 1). It would be obvious to combine the power PC bus with Chan, because the power PC bus is well-known bus master standard, and well recognized alternative embodiment of such. Therefore it would be obvious to one of ordinary skill in the art to combine a particular bus standard with Chan at the time the invention was made to obtain the claimed invention.

Regarding claim 6, Chan also discloses wherein the active module executes the memory write operation to the second memory, via the D-channel, and each of a primary D-channel controller and a secondary D-channel controller executes a duplexing operation (e.g., paragraph [0040]). While Chan does not expressly mention a particular embodiment of the power PC (PPC) bus, the Examiner takes Official Notice that this is a well-known bus master standard as further evidenced by Shaffer. Shaffer discloses the well-known power PC bus (e.g., col. 4, lines 51-55, Figure 1). It would be obvious to combine the power PC bus with Chan, because the power PC bus is well-known bus master standard, and well recognized alternative embodiment of such. Therefore it would be obvious to one of ordinary skill in the art to combine a particular bus standard with Chan at the time the invention was made to obtain the claimed invention.

Response to Arguments

Applicant's arguments filed 5/14/2004 have been fully considered but they are not persuasive.

Rejection of claim 16 under Jung was improper however and is withdrawn.

Regarding claim 17, Applicant argues that Jung "does not disclose a channel which conveys status signals for performing a duplexing operation" (p. 14); however, Jung discloses "[t]he operation mode is determined by the memory switch controller 440, and control signals "Enable_A, "Dir_A", "Enable_B, "Dir_B, "Enable_C, and "Dir_C" for controlling the active module memory switch 410, [and] the concurrent write memory switch 420" (col. 7, lines 51-58). Depending

on which module is the active module, these switches will necessarily operate accordingly and thus are determined to support a duplexing operation.

Applicant further argues that Jung "does not disclose a "channel [that] carries status signals between the modules" (p. 14); however as stated supra, these status signals are clearly disclosed in the citation of Jung.

Applicant further argues that "Jung expressly discloses that these signals are generated by controller 440 to control switches 410, 420, and 430 for the purpose of conveying data between the modules" (p. 14); this is correct but does not distinguish Jung from the claimed invention inasmuch as these are the status signals.

Applicant further argues that "these signals are used to control the conveyance of data over the data channel" (p. 15); however this in no manner prevents them from being interpreted as status signals.

Regarding claim 18, Applicant argues that Jung does not disclose an active status "identified by a true state existing on the self-side normal signal and a false state existing on the pair-side active signal"; however the cited passage discloses status signals that indicate a true state on the self-side normal signal and a false state on the pair-side active signal. At the cited passage, Jung discloses the status signals that indicate the active signal on the self-side normal signal. These signals subsequently mediate the correct propagation of data to the pair-side memory.

Regarding claim 22, Applicant argues that Jung does not disclose "setting one of the first and second devices to an active mode status and the other of the

respective devices to a standby mode status based on the first and second status, wherein both the first status and the second status are identified by a self-side normal signal and a pair-side active signal" (pp. 15-16); however the cited passage in Jung discloses precisely this: "The memory switch control signal generating part 442 serves to generate control signals which control the direction of the memory switch *in accordance with the control signals 'active mode', 'standby mode', 'standby module read' received from the operation mode determining part 441 and the control signal 'memory read' received from said memory controller 110*" (col. 8, lines 50-58).

Regarding claim 23, Applicant argues that Jung does not disclose at least a pair-side active signal; however this is clearly disclosed at the cited passage as detailed supra.

Regarding claim 24, Applicant argues that Jung "does not disclose the C-channel and C-channel controllers" (p. 16); however Jung discloses this at the cited passage. Further, Jung discloses "[t]he operation mode is determined by the memory switch controller 440, and control signals "Enable_A, "Dir_A", "Enable_B, "Dir_B, "Enable_C, and "Dir_C" for controlling the active module memory switch 410, [and] the concurrent write memory switch 420" (col. 7, lines 51-58). Depending on which module is the active module, these switches will necessarily operate accordingly and thus are determined to provide the active mode status of the channel as claimed.

Thus the rejection of claims 17-19 and 22-24 is maintained.

Regarding claim 1, Applicant argues that Chan does not disclose "a C-channel that exchanges the primary and secondary status information between the primary and secondary C-channel controllers to support duplexing logic between the active module and the standby module" (p. 17); however that is clearly the function of the figure element cited supra. That element, "248A" of Figure 5A, sends and receives logic information between the duplex unit regarding the failure state of either one; clearly this anticipates the claimed limitation.

Applicant further argues that Chan does not disclose "primary and secondary status information ... which are used to support duplexing logic between active and standby modules" (p. 17); however, as stated supra, the failure state of a unit is considered logic and its use in Chan makes it a form of duplexing logic; namely, if the primary unit fails, the second unit becomes active: this is a form of duplexing logic.

Regarding claim 5, Applicant argues that Chan "does not disclose a C-channel of this type"; however as cited supra, Chan clearly discloses the limitations of the C-channel as claimed.

Regarding claim 17, Applicant argues that Chan does not disclose the C-channel and C-channel controllers recited in this claim; however as stated supra, Chan discloses the C-channel and controllers as citations make clear.

Regarding claims 22 and 23, Applicant argues that Chan does not disclose the sideband signals to include the pair-side active signal; however, as cited, Chan discloses "the processor 219 writes the bit pattern into the register of

the memory controller 224 at system initialization or during a switchover of control from the master I/O control logic unit 212A to the slave I/O control logic unit 212B, and the like" (para. 47).

Thus the rejection of claims 1-3, 5, and 7-24 using Chan is maintained.

Regarding claim 1, Applicant argues that "Hammersley does not teach or suggest the features of claim 1 missing from Jung, e.g., a C-channel that exchanges the primary and secondary status information between the primary and secondary C-channel controllers to support duplexing logic"; however, Hammersley is not relied upon for this feature. Rather, Jung discloses "[t]he operation mode is determined by the memory switch controller 440, and control signals "Enable_A, "Dir_A", "Enable_B, "Dir_B, "Enable_C, and "Dir_C" for controlling the active module memory switch 410, [and] the concurrent write memory switch 420" (col. 7, lines 51-58). Depending on which module is the active module, these switches will necessarily operate accordingly and thus are determined to support duplexing logic.

Regarding claims 5, 18, 20, and 21, Applicant reiterates the assertion that the C-channel and C-channel controller are not disclosed by Jung (pp. 20-21); however, as explained supra, the C-channel as claimed is anticipated. No recitation of the channel distinguishes from this interpretation.

Thus the rejection of claims 1-3, 5, 20-21 using Jung in view of standard PCI bus mastering is maintained.

Regarding claims 4 and 6, Applicant argues that Shaffer does not disclose a C-channel; however, as previously stated, Jung is relied upon for this limitation.

Thus the rejection of claims 4 and 6 using Jung in view of standard bus mastering is maintained.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H Knoll whose telephone number is 703-305-8656. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

chk

Khanh Dang
Primary Examiner